



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE APPLICATION OF:

WILLIAM J. BORLAND

CASE NO.: **EL0509 US NA**

APPLICATION NO.:

CONFIRMATION NO.:

GROUP ART UNIT:

EXAMINER:

FILED: **HEREWITH**

FOR: **METHOD OF MAKING INNERLAYER PANELS AND PRINTED WIRING
BOARDS USING X-RAY IDENTIFICATION OF FIDUCIALS**

SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with 37 CFR 1.97 and 1.98, Applicants bring to the attention of the U.S. Patent and Trademark Office information listed on the enclosed PTO/SB/08. A copy of the information is also enclosed.

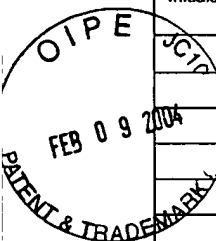
Should any fee be required in connection with the filing of this Information Disclosure Statement, please charge such fee to Deposit Account No. 04-1928 (E. I. du Pont de Nemours and Company).

Respectfully submitted,

REBECCA W. TULLOCH
ATTORNEY FOR APPLICANT
Registration No.: 36,297
Telephone: (302) 892-7911
Facsimile: (302) 992-7343

Dated: 2/5/04

Enclosures

**Complete if Known**

(Use as many sheets as necessary)

Sheet	1	of	3
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Application Number	10/718,044
Filing Date	November 20, 2003
First Named Inventor	William J. Borland
Art Unit	
Examiner Name	
Attorney Docket Number	EL0509 US NA

[illegible]

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	MM-DD-YYYY			
		JP 2003-92460	05-31-2002			
		JP 2-153589	06-13-1990	Ibiden KK		
		JP 2001-168491	12-09-1999			

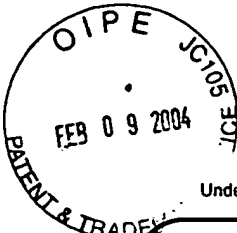
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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete If Known	
				Application Number	10/718,044
				Filing Date	November 20, 2003
				First Named Inventor	William J. Borland
				Art Unit	
				Examiner Name	
Sheet	2	of	3	Attorney Docket Number	EL0509 US NA

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
		JOHN FELTEN AND SAUL FERGUSON, Embedded Ceramic Resistors and Capacitors for PWB, IP Printed Circuit Expo, San Diego, CA, April 2000.	<input type="checkbox"/>	
		JOHN J. FELTEN AND SAUL FERGUSON, Ceramic Resistors and Capacitors Embedded in PWB, IPC, San Diego, April 5, 2000.	<input type="checkbox"/>	
		JOHN J. FELTEN AND SAUL FERGUSON, Ceramic Resistors and Capacitors Embedded in PWB, IMAPS, Denver, April 29, 2000.	<input type="checkbox"/>	
		JOHN J. FELTEN AND WILLIAM J. BORLAND, Embedded Ceramic Passives in PWB: Process Development, IPC Printed Circuit Expo, Anaheim, CA, April 2001.	<input type="checkbox"/>	
		JOHN J. FELTEN AND WILLIAM J. BORLAND, Ceramic Resistors and Capacitors Embedded in PWB's, IPC Expo, April 3, 2001.	<input type="checkbox"/>	
		WILLIAM BORLAND, Designing for Embedded Passives, Printed Circuit Design, August 2001.	<input type="checkbox"/>	

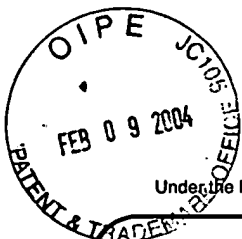
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PTO/SB/08b (08-03)

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Sheet 3 of 3

Complete If Known

Application Number	10/718,044
Filing Date	November 20, 2003
First Named Inventor	William J. Borland
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Examiner Name	
Attorney Docket Number	EL0509 US NA

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		DR. KIM FJELDSTED AND STACEY L. CHASE, Embedded Passives: Laser Trimmed Resistors, CircuitTree, Volume 70, March 2002.	<input type="checkbox"/>
		WILLIAM J. BORLAND AND SAUL FERGUSON, Embedded Passive Components in Printed Wiring Boards, a Technology Review, To be published in CircuitTree Magazine, 2001.	<input type="checkbox"/>
		JIMING ZHOU, JOHN D. MYERS AND JOHN J. FELTEN, Embedded Passives Technology for PCBs: Materials, Design, and Process, IMAPS 2002 Conference, Denver, CO, Sept. 4-6, 2002.	<input type="checkbox"/>
		JOHN J. FELTEN, Electronic Circuits World Convention, Paper number IPC31, Advanced Embedded Passives Technologies - Putting Ceramic Components into Organic PWBs.	<input type="checkbox"/>
		WILLIAM BORLAND, JOHN J. FELTEN, SAUL FERGUSON, ALTON B. JONES AND ANGELA A. LAWRENCE, Embedded Singulated Ceramic Passives in Printed Wiring Boards, IMAPS Advanced Technology Workshop on Passive Integration, Ogunquit, ME, June 19-21, 2002.	<input type="checkbox"/>
		RICHARD C. SNOGREN, Embedded Passives, a Review, IPC Designers Learning Symposium, October 3, 2002, Toronto ON, CN.	<input type="checkbox"/>

Examiner Signature		Date Considered	
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10/718,044

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